**SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**

**Ramapuram Campus, Bharathi Salai, Ramapuram,**

**Chennai - 600089**

**FACULTY OF ENGINEERING AND TECHNOLOGY**

# DEPARTMENT OF

# COMPUTER SCIENCE AND ENGINEERING

****

**QUESTION BANK**

**DEGREE / BRANCH: B Tech/CSE and all specializations**

**(AIML, BDA, IOT, CS)**

**III SEMESTER**

**18CSC203J**-**COMPUTER ORGANIZATION AND ARCHITECTURE**

**Regulation–2018**

**Academic Year -2021-2022**

**SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**

**Ramapuram Campus, Bharathi Salai, Ramapuram, Chennai-600089**

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

**QUESTION BANK**

**SUBJECT CODE : 18CSC203J**

**SUBJECT NAME : COMPUTER ORGANIZATION AND ARCHITECTURE**

**SEM/YEAR:III/II**

**Course Outcomes**

***CO1:*** *Identify the computer hardware and how software interacts with computer hardware*

***CO2:*** *Apply Boolean algebra as related to designing computer logic, through simple combinational and sequential logic circuits*

***CO3:*** *Analyze the detailed operation of Basic Processing units and the performance of Pipelining*

***CO4:*** *Analyze concepts of parallelism and multi-core processors*

***CO5:*** *Identify the memory technologies, input-output systems and evaluate the performance of memory system*

***CO6:*** *Identify the computer hardware, software and its interactions*

| **UNIT V** | | | |
| --- | --- | --- | --- |
| Memory systems -Basic Concepts, Memory hierarchy- Memory technologies, RAM, Semiconductor RAM- ROM,Types, Speed,size cost- Cache memory, Mapping Functions- Replacement Algorithms, Problem Solving- Virtual Memory, Performance considerations of various memories- Input Output Organization, Need for Input output devices- Memory mapped IO, Program controlled IO- Interrupts-Hardware, Enabling and Disabling Interrupts, Handling multiple Devices | | | |
| **PART-A (Multiple Choice Questions)** | | | |
| **Q.**  **No** | **Questions** | **Course Outcome** | **Competence**  **BT Level** |
| **1** | Which of the following is the smallest entity of memory?  (a) Block  **(b) Cell**  (c) Instance  (d) Set | CO5 | BT2 |
| **2** | The primary memory (also called main memory) of a personal computer consists of  (a) RAM only  (b) ROM only  **(c) both RAM and ROM**  (d) Cache memory | CO5 | BT1 |
| **3** | The Boot sector files of the system are stored in which computer memory?  (a) RAM  **(b) ROM**  (c) Cache  (d) Register | CO5 | BT2 |
| **4** | Which of the following statements are not correct about the main memory of a computer?  (a) In main memory, data gets lost when power is switched off.  (b) Main memory is faster than secondary memory but slower than registers.  (c) They are made up of semiconductors.  **(d) SRAM is used in Main memory** | CO5 | BT2 |
| **5** | What is the full form of RAM?  (a) Read Access Memory  **(b) Random Access Memory**  (c) Readable Access Memory  (d) Random Accumulator Memory | CO5 | BT1 |
| **6** | RAM is \_ \_ \_ \_ \_ \_ and \_ \_ \_ \_ \_.  **(a) volatile, temporary**  (b) non-volatile, temporary  (c) volatile, permanent  (d) non-volatile, permanent | CO5 | BT3 |
| **7** | Which of the following memory is non-volatile?  (a) RAM  **(b) ROM**  (c) Cache  (d) ROM and Cache | CO5 | BT2 |
| **8** | Which of the following is the lowest in the computer memory hierarchy?  (a) Cache  (b) RAM  **(c) Secondary memory**  (d) CPU registers | CO5 | BT2 |
| **9** | Which of the following has the fastest speed in the computer memory hierarchy?  (a) Cache  **(b) Register in CPU**  (c) Main memory  (d) Disk cache | CO5 | BT1 |
| **10** | Which memory acts as a buffer between CPU and main memory?  (a) RAM  (b) ROM  **(c) Cache**  (d) Storage | CO5 | BT2 |
| **11** | Which of the following statements are not correct about cache memory?  (a) Cache memory is used to store data temporarily.  (b) It holds that data and program which has to be executed within a short period of time.  **(c) It needs frequent refreshing**  (d) It consumes less access time as compared to the Main memory | CO5 | BT2 |
| **12** | In which type of ROM, data can be erased by ultraviolet light and then reprogrammed by the user or manufacturer?  (a) PROM  (b) **EPROM**  (c) EEPROM  (d) Both a and b | CO5 | BT1 |
| **13** | Primary storage is . . . . . . . as compared to secondary storage.  (a) Slow and inexpensive  (b) Fast and inexpensive  **(c) Fast and expensive**  (d) Slow and expensive | CO5 | BT2 |
| **14** | Which of the following statements is not true about secondary memory (auxiliary memory)?  (a) Secondary memory is non-volatile in nature and slower than primary memories.  **(b) It is a faster memory device**  (c) Data is permanently stored even if power is switched off.  (d) Computers may run without secondary memory.  (e) It is also known as backup memory. | CO5 | BT2 |
| **15** | Virtual memory is an  (a) Extremely large memory  (b) Extremely large secondary memory  **(c) Illusion of an extremely large memory**  (d) A type of memory used in supercomputers. | CO5 | BT2 |
| **16** | Whenever the data is not found in the cache memory it is called as \_\_\_\_\_\_\_\_\_  a) HIT  **b) MISS**  c) FOUND  d) ERROR | CO5 | BT2 |
| **17** | When the data at a location in cache is different from the data located in the main memory, the cache is called \_\_\_\_\_\_\_\_\_\_\_\_\_  a) Unique  **b) Inconsistent**  c) Variable  d) Fault | CO5 | BT2 |
| **18** | Which of the following is not a write policy to avoid Cache Coherence?  a) Write through  **b) Write within**  c) Write back  d) Buffered write | CO5 | BT2 |
| **19** | In \_\_\_\_\_\_\_\_\_\_\_\_ mapping, the data can be mapped anywhere in the Cache Memory.  **a) Associative**  b) Direct  c) Set Associative  d) Indirect | CO5 | BT2 |
| **20** | The transfer between CPU and Cache is \_\_\_\_\_\_\_\_\_\_\_\_\_\_  a) Block transfer  **b) Word transfer**  c) Set transfer  d) Associative transfer | CO5 | BT2 |
| **21** | LRU stands for \_\_\_\_\_\_\_\_\_\_\_  a) Low Rate Usage  b) Least Rate Usage  **c) Least Recently Used**  d) Low Required Usage | CO5 | BT1 |
| **22** | The binary address issued to data or instructions are called as \_\_\_\_\_\_  a) Physical address  b) Location  c) Relocatable address  **d) Logical address** | CO5 | BT1 |
| **23** | Which of the following is not the main aim of virtual memory organization?  a) To provide effective memory access  **b) To provide permanent backup**  c) To improve the execution of the program  d) To provide better memory transfer | CO5 | BT1 |
| **24** | TLB is a \_\_\_\_\_\_\_   1. Permanent memory 2. Larger memory 3. **Small cache** 4. Interface used for I/O devices | CO5 | BT1 |
| **25** | Which of the following is used for detecting and correcting errors?   1. ACC 2. BCC 3. **ECC** 4. TLB | CO5 | BT1 |
| **26** | In a 3.5 inch(diameter) capacity magnetic disk, There are an average of \_\_\_\_\_\_sectors per track   1. 200 2. 300 3. **400** 4. 500 | CO5 | BT2 |
| **27** | Which of the following is the time required to move the read/write head to the proper track?   1. Track time 2. Fetch time 3. **Seek time** 4. Disk time | CO5 | BT1 |
| **28** | ROM stores a small \_\_\_\_\_\_ program that can read and write main memory locations   1. **monitor** 2. snooping 3. writer 4. sub-routine | CO5 | BT1 |
| **29** | In memory design, an approach to implement a narrow bus that is much faster is \_\_\_\_\_\_   1. **Rambus** 2. internal bus 3. Memory bus 4. multi bus | CO5 | BT1 |
| **30** | After the completion of the DMA transfer, the processor is notified by \_\_\_\_\_\_\_\_\_\_  a) Acknowledge signal  **b) Interrupt signa**l  c) WMFC signal  d) None of the mentioned | CO5 | BT1 |
| **31** | How is a privilege exception dealt with?  **a) The program is halted and the system switches into supervisor mode and restarts the program execution**  b) The Program is stopped and removed from the queue  c) The system switches the mode and starts the execution of a new process  d) The system switches mode and runs the debugger | CO5 | BT1 |
| **32** | The instructions which can be run only supervisor mode are?  a) Non-privileged instructions  b) System instructions  **c) Privileged instructions**  d) Exception instructions | CO5 | BT2 |
| **33** | The two facilities provided by the debugger is \_\_\_\_\_\_\_\_\_\_  a) Trace points  b) Break points  c) Compile  **d) Both Trace and Break points** | CO5 | BT2 |
| **34** | If during the execution of an instruction an exception is raised then \_\_\_\_\_\_\_\_\_\_  a) The instruction is executed and the exception is handled  **b) The instruction is halted and the exception is handled**  c) The processor completes the execution and saves the data and then handle the exception  d) None of the mentioned | CO5 | BT2 |
| **35** | Interrupts initiated by an instruction is called as \_\_\_\_\_\_\_  a) Internal  **b) External**  c) Hardware  d) Software | CO5 | BT2 |
| **36** | In memory-mapped I/O \_\_\_\_\_\_\_\_\_\_\_\_  **a) The I/O devices and the memory share the same address space**  b) The I/O devices have a separate address space  c) The memory and I/O devices have an associated address space  d) A part of the memory is specifically set aside for the I/O operation | CO5 | BT3 |
| **37** | The advantage of I/O mapped devices to memory mapped is \_\_\_\_\_\_\_\_\_\_\_  a) The former offers faster transfer of data  b) The devices connected using I/O mapping have a bigger buffer space  **c) The devices have to deal with fewer address lines**  d) No advantage as such | CO5 | BT2 |
| **38** | The system is notified of a read or write operation by \_\_\_\_\_\_\_\_\_\_\_  a) Appending an extra bit of the address  b) Enabling the read or write bits of the devices  c) Raising an appropriate interrupt signal  **d) Sending a special signal along the BUS** | CO5 | BT2 |
| **39** | To overcome the lag in the operating speeds of the I/O device and the processor we use \_\_\_\_\_\_\_\_\_\_\_  a) Buffer spaces  **b) Status flags**  c) Interrupt signals  d) Exceptions | CO5 | BT1 |
| **40** | The method which offers higher speeds of I/O transfers is \_\_\_\_\_\_\_\_\_\_\_  a) Interrupts  b) Memory mapping  c) Program-controlled I/O  **d) DMA** | CO5 | BT2 |
| **41** | The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is?  a) Exceptions  b) Signal handling  **c) Interrupts**  d) DMA | CO5 | BT2 |
| **42** | The process wherein the processor constantly checks the status flags is called as \_\_\_\_\_\_\_\_\_\_\_  **a) Polling**  b) Inspection  c) Reviewing  d) Echoing | CO5 | BT2 |
| **43** | How can the processor ignore other interrupts when it is servicing one \_\_\_\_\_\_\_\_\_\_\_  a) By turning off the interrupt request line  b) By disabling the devices from sending the interrupts  c) BY using edge-triggered request lines  **d) All of the mentioned** | CO5 | BT1 |
| **44** | CPU as two modes privileged and non-privileged. In order to change the mode from privileged to non-privileged.  a) A hardware interrupt is needed  **b) A software interrupt is needed**  c) Either hardware or software interrupt is needed  d) A non-privileged instruction (which does not generate an interrupt)is needed | CO5 | BT2 |
| **45** | An interrupt that can be temporarily ignored is \_\_\_\_\_\_\_\_\_\_\_  a) Vectored interrupt  b) Non-maskable interrupt  **c) Maskable interrupt**  d) High priority interrupt | CO5 | BT1 |
| **46** | The time between the receiver of an interrupt and its service is \_\_\_\_\_\_  a) Interrupt delay  **b) Interrupt latency**  c) Cycle time  d) Switching time | CO5 | BT2 |
| **47** | When the process is returned after an interrupt service \_\_\_\_\_\_ should be loaded again.  i) Register contents  ii) Condition codes  iii) Stack contents  iv) Return addresses  a) i, iv  b) ii, iii and iv  c) iii, iv  **d) i, ii** | CO5 | BT2 |
| **48** | The signal sent to the device from the processor to the device after receiving an interrupt is \_\_\_\_\_\_\_\_\_\_\_  **a) Interrupt-acknowledge**  b) Return signal  c) Service signal  d) Permission signal | CO5 | BT2 |
| **49** | The return address from the interrupt-service routine is stored on the \_\_\_\_\_\_\_\_\_\_\_. a) System heap  b) Processor register  **c) Processor stack**  d) Memory | CO5 | BT1 |
| **50** | The interrupt-request line is a part of the \_\_\_\_\_\_\_\_\_\_\_. a) Data line  **b) Control line**  c) Address line  d) None of the mentioned | CO5 | BT2 |
| **PART B (4 Marks)** | | | |
| **1** | Write on address spaces in I/o Devices with a neat diagram. | CO5 | BT1 |
| **2** | Treatment of an interrupt-service routine is very similar to that of a subroutine –Justify the above statement | CO5 | BT3 |
| **3** | Does Saving and restoring registers involve memory transfers? Is the statement true or false .explain in brief your answer? | CO5 | BT2 |
| **4** | What are the steps to be done to reduce interrupt latency? | CO5 | BT2 |
| **5** | Write short notes Delay, latency and interrupt latency. | CO5 | BT2 |
| **6** | Define hardware interrupt. | CO5 | BT1 |
| **7** | Draw a diagram for enabling and disabling of interrupts? | CO5 | BT2 |
| **8** | Explain on privilege exception? | CO5 | BT2 |
| **9** | Explain about speed size cost? | CO5 | BT2 |
| **PART C (12 Marks)** | | | |
| **1** | Write on privilege exception and draw a diagram to justify your answer and explain it. | CO5 | BT2 |
| **2** | Difference between handling I/O interrupt-request and handling exceptions due to errors and brief on it. | CO5 | BT2 |
| **3** | Discuss in detail about the Control unit which performs these transfers is a part of the I/O devices**.** | CO5 | BT2 |
| **4** | Draw and explain DMA bus attribution .Converse on your answer with your own example | CO5 | BT3 |
| **5** | Draw a diagram with master and slave for your synchronous bus and describe on it**.** | CO5 | BT3 |